Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-24. (canceled)

25. (previously presented) A device comprising:

an integrated circuit chip having a plurality of contact pads ~~dimensioned smaller than 50 μm across and spaced apart less than 100 μm center to center~~;

a single-layered insulating ~~thin film~~ interposer ~~having a single layered insulating~~ film having a top surface and a bottom surface;

~~substantially flat,~~ an electrically conductive ~~lines~~ pattern formed of a conductive film disposed on ~~only one side~~ the top surface of the insulating film;

~~electrically conductive paths~~ vias extending through the interposer filled with conductive material, contacting the conductive [[lines]] pattern, and forming exit ports on ~~a second side of the insulating film~~ the bottom surface;

the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad; and

thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer.

26. (previously presented) The device of claim 25, further comprising solder balls attached to the exit ports.

27. (previously presented) The device of claim 25, further comprising encapsulating material encapsulating the integrated circuit chip.

28. (new) A substrate for connecting an integrated circuit chip having a plurality of contact pads, comprising:

a single-layered insulating interposer film having a top surface and a bottom surface;

an electrically conductive pattern formed of a conductive film disposed on the top

surface of the insulating interposer film;

vias extending through the interposer, filled with conductive material, contacting the conductive pattern, and forming exit ports on the bottom surface; and

the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad.

29. (new) The substrate in claim 28, further comprising solder balls attached to the exit ports.

30. (new) The substrate in claim 28, in which the conductive pattern includes attachment sites corresponding to contact pads on the integrated circuit chip.

31. (new) A device comprising a substrate in claim 28, and an integrated chip attached to the substrate.

32. (new) A BGA substrate having a top surface and a bottom surface;

the top surface having a conductive pattern including attachment sites for attaching an integrated circuit chip;

vias extending through the substrate, filled with conductive material, forming exit ports at the bottom surface;

the bottom surface free of conductive material, except solder material at the exit ports electrically connected to the conductive material in the vias.

33. (new) A BGA device comprising a substrate in claim 32 and an integrated circuit chip attached thereon.

34. (new) The BGA device of claim 33, in which the integrated circuit is encapsulated with an encapsulating material.

35. A BGA substrate comprising

a top surface having a conductive pattern including attachment sites for attaching an integrated circuit chip; and a insulating bottom surface;

vias extending through the substrate, filled with conductive material, forming exit

ports at the bottom surface; and

solder material at the exit ports electrically connected to the conductive material in the vias.

36. (new) A BGA device comprising a substrate in claim 35 and an integrated circuit chip attached thereon.

37. (new) The BGA device of claim 36, in which the integrated circuit is encapsulated with an encapsulating material.